

THE EMBODIMENTS OF THE INVENTION IN WHICH AN EXCLUSIVE PROPERTY OR PRIVILEGE IS CLAIMED ARE DEFINED AS FOLLOWS:

1. A memory board for use in a memory subsystem of a data processing system, said memory subsystem performing memory operations, such as reading and writing, and including a system bus interface unit and a memory unit bus, said memory unit bus being coupled to said memory board and at least one additional memory board, and said memory board comprising:

a plurality of storage cell array means for storing data signal groups;

array bus means coupled to each of said storage cell array means, for transferring signals with each of said storage cell array means;

sequencer means, coupled to said array bus means, for controlling the memory operations of each of said storage cell array means and for receiving ready signals from each of said storage cell array means via said array bus means, said ready signals indicating the impending completion of a current one of said memory operations, and said sequencer means including apparatus for generating, from the ready signals received from said array bus means, a first signal prior to the time when said storage cell array means <sup>has</sup> completed its current memory operation; and

interface means, coupled to said sequencer means, for applying said first signal and a second signal to said system bus interface unit, said second signal indicating that said ~~at least~~ ~~one~~ storage cell array means can process no commands.

2. The memory board of Claim 1 wherein said memory board can perform the memory operations at a speed independent of said at least one additional memory board coupled to said memory unit bus.

3. The memory board of Claim 1 further comprising an array bus for coupling said storage cell array means to said interface means.

4. The memory board of Claim 1 wherein said memory board further comprises;

buffer means coupled to each of said plurality of storage cell array means, for receiving data from said data processing system and for simultaneously processing a write operation to write said data in at least two of said plurality of said storage cell array means coupled to said memory board.

5. A memory board for operation in a main memory unit including a plurality of other memory boards, said memory board comprising:

storage means for processing data signals, by storing and retrieving said data signals in response to address and

command signals, concurrently with said other memory boards in said main memory unit, said storage means including

a plurality of memory array units each including

a plurality of storage cells for processing said data signals at locations corresponding to said address signals, and

means for processing said data signals in response to said address and command signals to effect storage of said data signals into and retrieval of said data signals from said storage cells concurrently with the processing of said data signals by other of said memory array units and for generating an array status signal indicating the impending availability of that memory array unit to process said data signals;

board status means, coupled to said storage means, for generating board status signals from said array status signals, said board status signals indicating the impending availability of said storage means to process said data signals; and

array bus means coupled to said plurality of memory array units, for transferring said command, data and address and array status signals between said board status means and each of said plurality of memory array units.

6. A memory board of Claim 5 wherein each said board status means includes board interface means, coupled to said array bus, for forming said board status signals from said array status signals.

7. A memory board according to Claim 5 wherein each of said memory array units also includes:

buffer means, coupled between said plurality of storage cells and said array bus means, for providing temporary storage of said data signals and said address signals, and

sequencing means, coupled between said array bus means and said plurality of storage cells, for controlling the processing of said storage cells in accordance with said command signals received from said array bus means and for providing said array status signals to said array bus means.

8. The memory board according to Claim 7 wherein said sequencing means includes means for generating said array status signals indicating completion of a processing operation by said storage cells.

9. A memory board according to Claim 6 wherein said board interface means includes means for generating said board status signals indicating completion of a processing operation by the associated board.

10. A memory board according to Claim 6 wherein said board interface means includes means for temporarily storing said address, command, data and board status signals.

11. A memory board according to Claim 5 wherein said data are stored at locations in said memory array units corresponding to said address signals, and wherein consecutive ones of said locations are distributed over said plurality of memory array units.

12. A memory board for use in a memory subsystem of a data processing system, said memory subsystem performing memory operations, such as reading and writing, and including a memory unit bus coupled to said memory board and to at least one additional memory board, and said memory board comprising: a plurality of storage cell array means for storing data signal groups; array bus means, coupled to each of said storage cell array means, for transferring signals with each of said storage cell array means; a plurality of sequencer means, each being coupled to said array bus means and to a corresponding one of said storage cell array means, for controlling the memory operations of the corresponding one of said storage cell array means and for placing onto said array bus means done signals indicating the impending completion of a current one of said memory operations; and interface means, coupled to said array bus means, for combining said done signals from said plurality of sequencer means into a ready/done signal prior to the time when said storage cell array means have completed their current memory operations and for applying said ready/done signal and a second signal to said memory unit bus, said second signal indicating that said memory board can process no commands.

13. The memory board of Claim 12, wherein said at least one storage cell array means includes a plurality of storage array means and wherein said memory board further comprises: an array bus means for distributing signals to said plurality of storage cell array means coupled to said memory board; and buffer means, coupled to each of said plurality of storage cell array means, for receiving data from said data processing system and for simultaneously processing a write operation to write said data in at least two of said plurality of said storage cell array means coupled to said memory board.

14. A memory board for operation in a main memory unit including a plurality of other memory boards, said memory board comprising: storage means for processing data signals by storing and retrieving said data signals in response to address and command signals concurrently with said other memory boards in said main memory unit, said storage means including a plurality of memory array units each including a plurality of storage cells for processing said data signals at locations corresponding to said address signals, and means for processing said data signals in response to said address and command signals to effect storage of said data signals into and retrieval of said data signals from said storage cells concurrently with the processing of said data signals by other of said memory array units, and for generating a done signal indicating the impending availability of that memory array unit to process said data signals; board status means for generating board status signals from said done signals, said board

status signals including ready/done signals being generated prior to the time when said storage cells have completed their processing operations and indicating the impending completion of said storage means' processing of data signals, and send no command signals indicating the availability of said memory board to process said data signals; and array bus means, coupled to said plurality of memory array units, for transferring said command, data, and address signals and said done signals between said board status means and each of said plurality of memory array units.

15. A memory board of Claim 14 wherein each said board status means includes board interface means, coupled to said array bus, for forming said board status signals from said done signals.

16. A memory board according to Claim 15 wherein said board interface means includes means for temporarily storing said address, command, data and board status signals.

17. A memory board according to Claim 14 wherein each of said memory array units includes: a plurality of storage cells for processing said data signals at locations corresponding to said address signals, buffer means, coupled between said plurality of storage cells and said array bus, for providing temporary storage of said data signals and said address signals, and sequencing means, coupled between said array bus and said plurality of storage cells, for controlling the processing of said storage cells in accordance with said command signals received from said

array bus and for providing said done signals to said array bus.

18. A memory board according to Claim 14 wherein said data signals are stored at locations in said memory array units corresponding to said address signals, and wherein consecutive ones of said locations are distributed over said plurality of memory array units.

SMART & BIGGAR  
OTTAWA, CANADA  
PATENT AGENTS

